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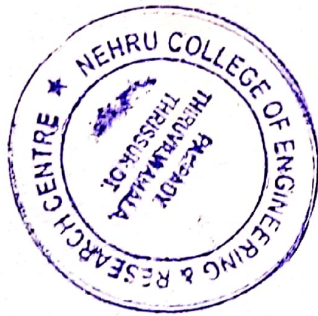
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3.3.3 No. of books and chapters in edited volumes/books published and papers published in national/international conference proceedings per teacher during last five years.

Academic Year	Page No
2019-2020	2
2018-2019	11
2017-2018	12
2016-2017	16
2015-2016	21



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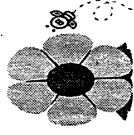
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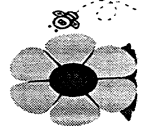
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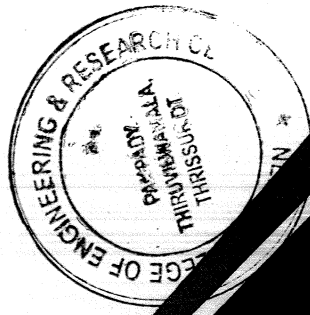


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**ULTRA LOW POWER QRS DETECTION AND ECG COMPRESSION
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An Advanced BIRA for Memories using Threshold Technique and Spare Allocation

Anjali Peradath *, Dr. S. Rajkumar **

* (PG Scholar, Department of Electronics and Communication Engineering, Nehru College of Engineering and Research Centre, Pampady, Thrissur, Kerala, India

** (Head of Dept., Department of Electronics and Communication Engineering, Nehru College of Engineering and Research Centre, Pampady, Thrissur, Kerala, India

ABSTRACT

The aim of this paper is to reduce the power consumption and timing with quick fault analysis and spare wire allocation. A common solution which is utilized to guarantee reasonable memory yields is built in redundancy analysis (BIRA). BIRA has two-dimensional spare architecture and is a module that stores and analyzes fault addresses. Numerous different parameters are considered when the performance of BIRA is evaluated such as repair rate, area overhead, and analysis speed. To reduce the area, power consumption and delay a new method of spare allocation using threshold technique is proposed in this paper. It focuses on a 100% repair rate and a minimal area overhead with reduced power consumption and timing. In the fault collection phase, the proposed BIRA identifies the total number and the location of the faults. After the fault collection phase, a redundancy analysis (RA) procedure is performed and the allocation is done with optimized spare wires. By doing so, the proposed BIRA algorithm can repair all repairable faulty memories while maintaining a minimal area overhead and reducing power consumption and delay.

Keywords - Analysis speed, Area overhead, BIRA, Delay, Fault addresses, Fault collection phase, Power consumption, Redundancy analysis, Repair rate, Spare allocation, Threshold technique, Two-dimensional spare architecture

Date of Submission: 29-08-2020

Date of Acceptance: 14-09-2020

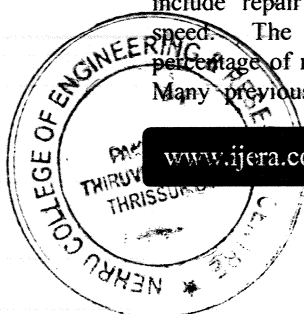
I. INTRODUCTION

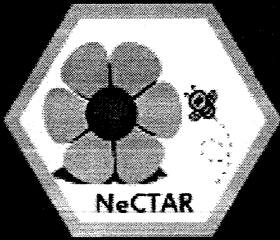
The recent rapid growth in the manufacturing of micro-semiconductors has facilitated substantial increases with regards to the memory density and capacity of these devices. As memory density has increased, so too has the chance of faults occurring within these memories. As this can lead to significant yield and reliability issues in semiconductor memories, appropriate solutions need to be found. One promising solution is built-in redundancy analysis (BIRA), which analyzes fault addresses that have been detected and repairs them with spare cells that were incorporated for this purpose. Typically, these redundant cells are incorporated in a two-dimensional spare line architecture comprising row spares and column spares, and the redundancy analysis (RA) for such cells is known to be NP-complete. As such, repair algorithms have to be carefully selected.

The typical performance criteria for BIRAs include repair rate, area overhead, and analysis speed. The repair rate is represented by the percentage of repaired chips in all repairable chips. Many previous BIRA algorithms have looked at

achieving a 100% repair rate because this criterion is directly related to the yield of memories. Area overhead is also important because the areas of chips are limited and larger area overhead leads to more expensive chips. Analysis speed, however, has recently been considered to be less important. Previous search-tree-based RA algorithms spent too much time on determining repair solutions because the search mechanisms for determining these solutions were exhaustive. One way of reducing this time was by reducing the analysis speed. However, recent BIRA approaches have used content addressable memories (CAMs) to achieve significant improvements in analysis speeds. As a result, most of the test and repair times of built-in self-repair (BISR) are taken up by the running of built-in self-test (BIST).

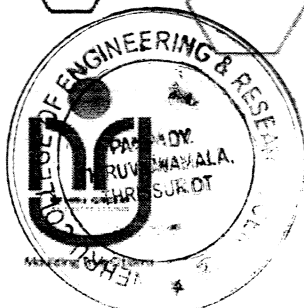
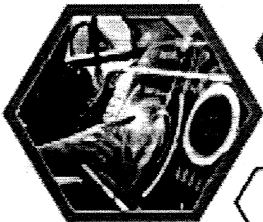
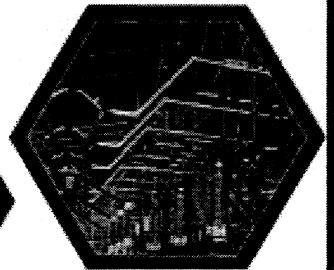
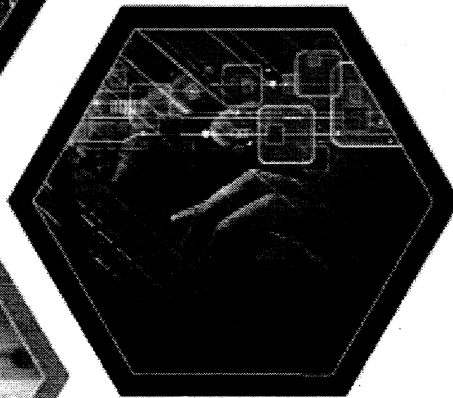
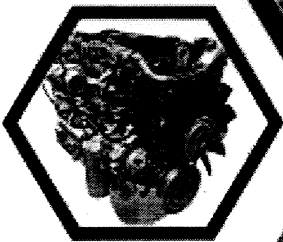
In the existing system, it focuses on dividing the faults into 2 categories: spare pivot fault and non-spare pivot fault. Here the fault collection and RA procedure takes a lot of time and hence the area and power consumption is very high. It becomes difficult to implement for large memories. Hence to remove the drawbacks of the existing BIRA approach a new technique has been introduced.





2020 PROCEEDINGS of Nehru e-Conference on Technologies Annexing Reality

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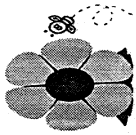
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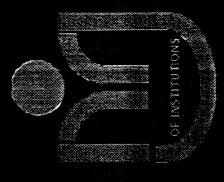
*Automatic Motor Vehicle Insurance Claims Process and Vehicle Damage Detection using Deep learning
in Nehru e-Conference on Technology Annexing Reality
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Automatic Motor Vehicle Insurance Claims Process and Vehicle Damage Detection using Deep learning.

Vineetha K R Asst. Professor ,MCA Dept.,NCERC

The Motor Vehicle Damage Insurance claims system is a set of Deep Learning algorithms with an API that utilizes computer vision. Based on deep learning, the algorithms automatically detect a vehicle's body and analyse the extent of the damage with automate the claim process for insurance. Deep learning allows for recognizing damaged vehicle parts, accessing insurance status, making predictions about what kind of repair is needed, and estimating how much cost it may claims.

Deep Learning has shown Promising results in Machine learning applications. Deep Learning is booming in every industry in the present market. This is because of its efficiency to reduce the manual work hours spent on a given problem. It automates the task by making the machine understand the problem to come up with a variety of solutions. The way it accomplishes this is by learning from the data we feed to it.

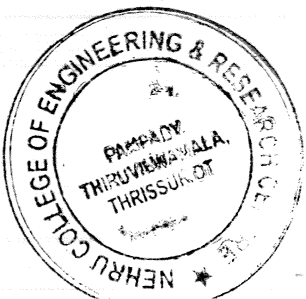
Today, in the vehicle insurance industry, a lot of money is wasted due to claim leakage. Visual Inspection and validation have been used to reduce such claims leakage. However, they delay to mitigate insurance claim processing.

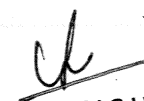
Insurance industries are getting digitised using these Deep Learning techniques, and are making our way of lives, a lot easier. The quickening of rendering services to the customers, detecting malicious activities, etc. are being done with a lot more ease than that has been done earlier. The latest advances in computer vision algorithms using deep learning are achieving interesting results in the classification of images, object detection, and image segmentation. The applications are still emerging, an increasing number of companies are starting to look at this technology as a way to make insurance claims processes easier and more efficient as one of the insurtech industry's biggest challenges.

Assessing the risk factors and accompanying them with the right price serves as an important factor in deciding the right insurance policy. Conventional techniques of looking into fewer affecting factors might not give a complete picture of which insurance to choose for the problem in hand. However, using Deep Learning, a number of patterns. Deep Learning provides a set of tools and techniques that take in humongous amounts of data, process it, and consolidate the results such as customer data, insurance claim, membership data, premiums and benefits provided, etc. This outputs precise results and reduces the losses incurred by executing the required set of actions, which in turn helps in fraud detection at an incredible rate.

Automatic Vehicle Damage detection:

Inspections are often the very first step of the car insurance claim process. With deep learning we can automatically detect scratches, dents, rust, breakages. We can also detect which part of the vehicle is damaged and with what severity. The vehicle can be automatically inspected using images or video feeds by creating a 360° overview. After the inspection, the report can be generated with a list of damages and estimate cost repair.




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This book can be described as bible for people who are invested in research and studies of HVDC, step up DC-DC converter. This adds a fresh perspective into the area of step up converter and HVDC. It simply blows the mind of people who are interested in innovative converters, available in the market. The author has dedicated his vast knowledge obtained through hands on experience in DC-DC step up converter. The book easily conveys the idea of converters and also explores the marvels of simple yet complicated understanding of HVDC.



Aswin Prakasan
Rajkumar Ganesa Moorthy

A High Efficiency Step-Up DC-DC Converter Combining KY And MMC

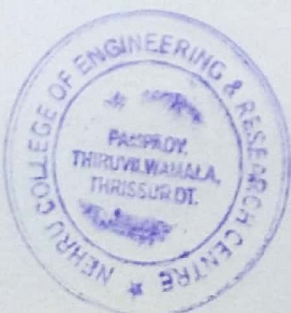


A novel step up converter is described, which combines the KY converter and the Multilevel Modular Converter (MMC). MMC is integrated to reduce the voltage and current stresses of switching device, improve efficiency, and fault-tolerant capability.



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This book gives a detailed knowledge about the importance and procedure in plastic waste disposal with complete detail and a working model developed to reduce the plastic wastes through pyrolysis, and along with that, it gives an exposure in hybrid power generation from biomass decomposition. So, it will be helpful for the students and researchers to gain knowledge about the automation based plastic waste management and hybrid power generation.



Rajkumar Ganesamoorthy



Mr. G. Rajkumar, having an academic experience of about 7 years in Nehru College of Engineering and Research Centre, Pampady, Thrissur, Kerala. Have published 25 journals in National and International conferences and have a deep knowledge in electrical machines, custom power devices, power quality. He have completed his M.tech in Dr.M.G.R University

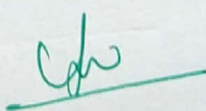
An Automated Hybrid Power Generation and Plastic Waste Management



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THEORY OF POWER ELECTRONIC DRIVES

P Sundaramoorthi
Prasana Moorthy
M. Murali
Vijayakumar .D



ISBN : 978-93-5311-277-6



MATLAB
exercises

PREFACE

We have great pleasure in introducing this text book “**THEORY OF POWER ELECTRONICS**” which covers as per the latest syllabus of All Technical Universities to serve as a text book for Undergraduate and Postgraduate students studying in Electrical and Electronics Engineering, Electronics and

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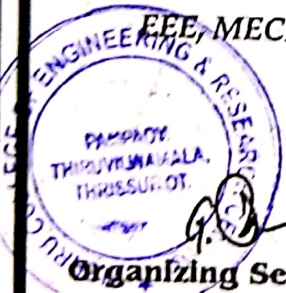
ENERGY TRANSFORMERLESS STEP-UP CONVERTER AND HB INVERTER TO

REDUCE LEAKAGE CURRENTS FOR GRID CONNECTED APPLICATIONS

in the 7th International Conference on Advanced Science and Engineering

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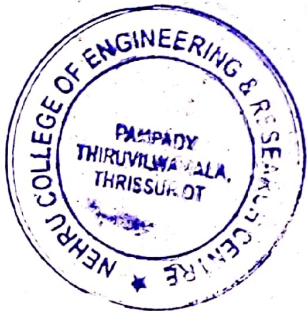
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EXERCISE : FROM CONTACT TO CONTACTLESS

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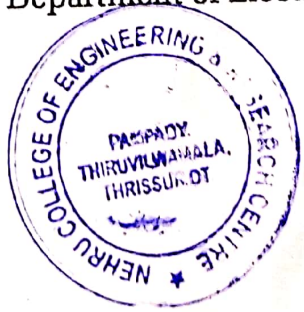
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in the National Conference on Innovative Strategies in Green & Soft computing for Renewable Energies- ISGSCRE '17, on

31st March 2017, Organized by Department of Electrical and Electronics Engineering, Sona College of Technology, Salem.

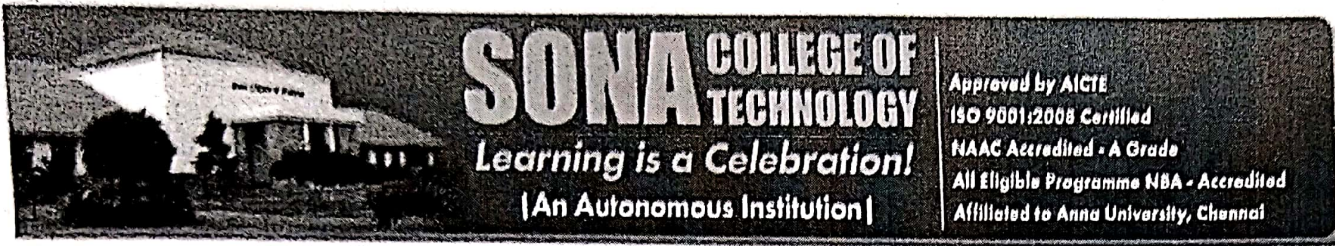
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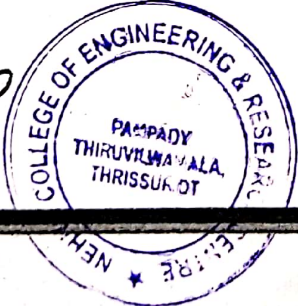


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The essential objective about vitality administration may be to process merchandise, furthermore give administrations with the any rate as cosset and slightest ecological impact. Those expression vitality administration methods a lot of people things will numerous individuals. The methodology of changing What's more upgrading energy, utilizing frameworks What's more methods thus Similarly as to decrease vitality necessities for every unit about yield same time holding steady alternately lessening downright costs from claiming generating the yield starting with these systems". Those destination for vitality oversaw economy may be with attain - what's more keep up ideal vitality acquisition, what's more utilization, all around the association and with minimize vitality fetches / waste without influencing preparation & quality, should minimize natural impacts. This book bargains with those essential data regards to the vitality preservation. Also review on a fast see from claiming destination sorts for inquires. It aids simple on realize those fundamental about vitality review.



Marudhai Vivek
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Vijayaraj S.

Energy Audit and Conservation (Objective Type)

Mr. M. Vivek is presently pursuing Ph.D / Research Associate in the Department of EEE/Mechanical Engineering, Periyar Maniammai University, Tamilnadu, India. He is having three years of industrial and research experience in the area of Renewable Energy. He has published a poetry book in Tamil language and Technical book for Engineering students.



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ICBG 2016

International Conference

Realm of Management in Bhagavad Gita

ON

4TH AND 5TH NOVEMBER, 2016

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 in the International Conference: Realm of Management in Bhagavad Gita organised by

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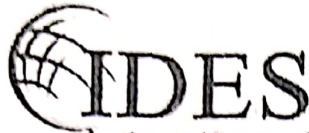
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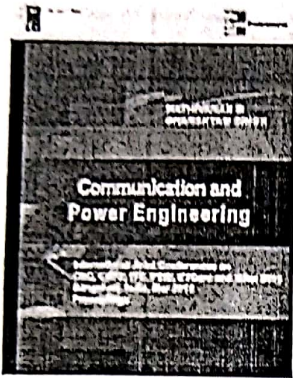
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Mathivanan B
Ghanshyam Singh (Eds.):

Communication and Power Engineering

IDES Joint International Conferences 2016

Held on : 12-13/03/16
place : Bangalore

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Usha and Kumuda D K

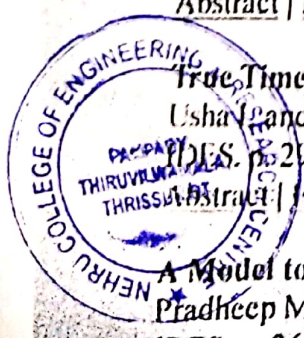
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Pradheep Manisekaran and Ashwin Dhivakar M R

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VLSI Design Of Efficient ML Detector For MIMO Wireless Communication Systems

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Abstract--

The complexity of modern wireless communication system are increasing at fast pace. So it is critical to verify the design characteristics at the earliest possible stage to minimize costly design iterations. The MIMO wireless communication system consists of MIMO transmitter and MIMO receiver along with the along with a realistic fading channel. Detection and performance analysis of the system, mainly BER measurement is done in the demodulation section. So far we have ML detectors with heavy hardware. Here an efficient ML detection algorithm is proposed for the MIMO signal detection based on differential metrics. ML detector with a control mechanism is proposed which can reduce the computational complexity. By reducing the number of multiplication operations, a low complexity ML algorithm, is proposed for efficient detection for MIMO wireless communication. The ML detector designed using VHDL coding, it is simulated in Model SIM 6.2b, synthesized using Xilinx ISE 13.1 for area and power analysis.

Index Terms— Additive white gaussian noise (AWGN), Bit-error rate (BER), Maximum likelihood (ML), Multiple input multiple output (MIMO).

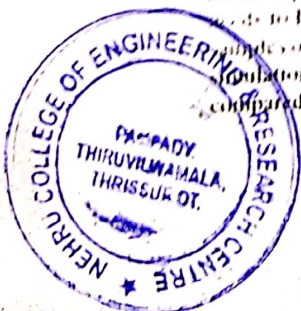
INTRODUCTION

The extensive demand for increasingly sophisticated connectivity anytime, anywhere, the wireless communication become one of the widest and rapidly growing field in telecommunication industry. MIMO transmission techniques become the significant advancement in wireless communication. And the complexity of modern wireless communication system are increasing at fast pace. It becomes challenging to design

the hardware of wireless system. But VLSI design techniques are nowadays capable of providing a powerful platform for those complicated designs.

1) Many modern techniques, such as multiple-input-multiple-output (MIMO) systems, rely on computationally intensive signal processing at the receiver. Therefore, bit-true software-based simulation of these algorithms on workstations is becoming prohibitively time consuming. In addition, for a communication system specification with a set of target system requirements such as data throughput, received power, available bandwidth, noise statistics, and a target error performance, there are typically various potential solutions. Each solution can use a different combination of subsystem designs with different sets of input parameters. Exploring the design space to achieve an optimized overall system solution that meets the target specifications can involve a large number of options.

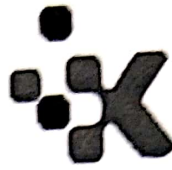
2) To estimate the BER performance of a communication system with the MC simulation method, we have to measure the BER over a large number of independent problem instances. While simulation of digital communication systems under additive white Gaussian noise (AWGN) channels is straightforward as the system performance is averaged over a large number of independent instances of noise and data, BER performance measurement of wireless systems over time-varying fading channels requires significantly longer simulation times because of the dependence between the channel instances. To accurately estimate the BER performance of a communication system over a time-varying fading channel, the error performance needs to be averaged not only on independent instances of noise and data, but also on the fading channel realizations over a long period. Such a performance evaluation can require several weeks or months of software simulations. Hardware simulators can accelerate the performance evaluation of communication systems compared with software simulators by several orders of magnitude.



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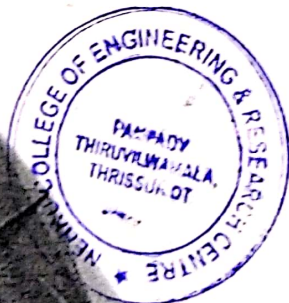
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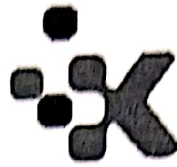


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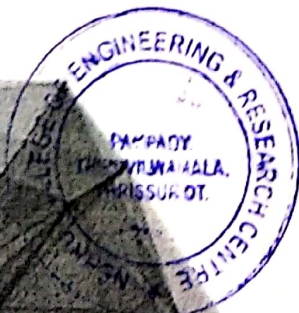
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Power Analysis of Various Modes of Multimode Architecture

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Abstract— Power consumption is one of biggest challenges in VLSI design. In the past, power has mainly been a concern for chips used in battery-powered devices. During long periods of inactivity, multi-threshold CMOS is very effective for reducing leakage power. There are many techniques to reduce static power. However, they are very much sensitive to process variations which affect manufacturability. Reducing leakage power remains to be one of the key design goals in the mean time. So, a new multi-mode power switch architecture with SPST adder as logic core is proposed. It offers greater power reduction and delay degradation and also requires less design effort. It also assures low leakage power and high tolerance to process variations. To achieve further static power reduction benefits, it can be combined with the existing techniques. Hence it is clear that the total power consumption can be decreased to a great extent using intermediate power off modes.

Index Terms— Multi-threshold CMOS (MTCMOS), Threshold Voltage (V_t), Leakage Current (IL), Spurious Power Suppression Technique (SPST), Most Significant Part (MSP), Least Significant Part (LSP).

I. INTRODUCTION

According to Moore's law, as chip density increases, power consumption is becoming a major problem for the contemporary systems [1]. There are two types of power: static and dynamic. Dynamic power can be reduced by the reduction of supply voltage level, since it is proportional to the square of supply voltage. But the execution time is adversely affected by this reduction. So, transistor threshold voltage is reduced, to maintain system performance. When threshold voltage is decreased, sub-threshold leakage current increases exponentially. So, for technologies below 90 nm, static power is so high that it is comparable in magnitude to dynamic power consumption.

A structure with intermediate power-off mode, which reduces the time required for recovering from idle mode at the expense of reduced leakage current suppression, is proposed. Similar structures were proposed by different authors. They extended this tradeoff between wake-up overhead and leakage power savings into multiple power-off modes. Hence the circuit is put into an intermediate power-off mode (i.e., low-power state), instead of consuming power by remaining in the

active mode during the short periods of inactivity, which is determined by the length of the idle period and the wake-up time. The higher are the power savings achieved when the period of inactivity is longer

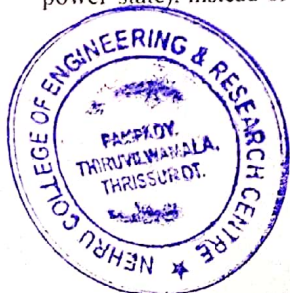
II. BACKGROUND

There are many techniques evolved for reducing leakage power. MTCMOS technology is effective for reducing the same. It is a variation of CMOS chip technology which has transistors with multiple threshold voltage to reduce delay and power. An approach is to use dual V_t libraries [3]. It suppresses leakage current, but reduces the performance.

Use of high V_t power switches between the circuit and power supply or ground rail can be used to decrease power [2], [3], [5]. During idle mode, these switches are turned off, there by suppressing leakage current. Its drawback is the large current rush during core reactivation and wakeup time. This limitation of power switches can be overcome by using intermediate power of modes. Wakeup time is the time required for recovering from idle mode. So, the circuit is put into a low power state or appropriate power of mode; instead of consuming power by remaining in the active mode [4]. Higher power savings can be achieved when the period of inactivity is longer, by using most aggressive power-off modes.

The previous architectures have several drawbacks. First, it cannot be easily extended to support more than two intermediate power-off modes and thus it cannot be used for high-performance circuits since the power reduction potential cannot be fully exploited. Next, a significant amount of power is consumed by the architecture and this reduces the advantages offered by the power switches. They are also very sensitive to process variations, which can affect its manufacturability and predictability adversely. Also, as it consists of analog components, it is not easily testable.

In this paper, we present an effective and robust multimode power-gating architecture that has none of the above drawbacks of the previous architectures. The proposed structure requires minimal design effort since it is very simple. It is considerably smaller and offers greater power savings for similar wake-up times.




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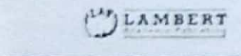
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